REMARKS

By this Amendment, Applicant has amended the specification to correct a typographical error. Applicant has also amended claims 1, 7, 12-14, 17, and 20 to more appropriately define the invention. Claim 16 has been canceled, without prejudice or disclaimer of the subject matter thereof. Claims 1-15 and 17-25 are pending.

In the Office Action, the Examiner rejected claims 1, 3-5, 12-13, 15, 20-21, and 23 under 35 U.S.C. § 102(b) as anticipated by Aiba et al. (U.S. Patent Pub. No. 2002/0190779 A1); rejected claims 20, 22, and 25 under 35 U.S.C. § 102(b) as anticipated by Fujita (U.S. Patent Pub. No. 2003/0020516 A1); rejected claims 1, 2, 7, 12, 13, 16, 19, and 25 under 35 U.S.C. § 102(a) as anticipated by Applicant's Prior Art ("APA") [1]; and rejected claims 6, 14, and 24 under 35 U.S.C. § 103(a) as unpatentable over Aiba et al. Claims 8-11 and 17-18 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

Applicant appreciates the indication of allowable subject matter. The rejection of claim 16 under 35 U.S.C. § 102(a) is rendered moot in view of the cancellation thereof. Applicant respectfully traverses the rejections of the remaining claims under 35 U.S.C. §§ 102 and 103(a).

In order to properly anticipate Applicant's claimed invention under 35 U.S.C. § 102, each and every element of the claim in issue must be found, "either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, "[t]he

[1] The detailed discussion of the Office Action indicates that the Examiner also rejected claims 19 and 25 under 35 U.S.C. § 102(a) as anticipated by APA. See Office Action, page 6.

identical invention must be shown in as complete detail as is contained in the . . . claim. Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)." See M.P.E.P. § 2131, 8th ed., Rev. of May 2004.

The rejection of claims 1, 3-5, 12-13, 15, 20-21, and 23 under 35 U.S.C. § 102(b) as anticipated by Aiba et al. should be withdrawn, because Aiba et al. does not teach each and every element of these claims.

Independent claim 1 recites a circuit for converting voltage levels that includes, inter alia, "a first power supply providing a first voltage level; a second power supply providing a second voltage level; a third power supply providing a third voltage level; . . . wherein a voltage level at a node disposed between the second transistor and the current source is pulled to the third voltage level in response to the first state of the input signal, and pulled to the second voltage level in response to the second state of the input signal."

The Examiner considered Aiba et al.'s power supply line 13 as corresponding to Applicant's claimed first power supply and Aiba et al.'s ground as corresponding to Applicant's claimed second power supply. See Office Action, page 2; see also Aiba et al., page 5, paragraph [0102], and Figs. 1, 2, and 17. However, Aiba et al. does not teach, at least, "a third power supply providing a third voltage level," as recited in claim 1. Consequently, Aiba et al. also fails to teach, at least, "wherein a voltage level at a node disposed between the second transistor and the current source is pulled to the third voltage level in response to the first state of the input signal, and pulled to the second voltage level in response to the second state of the input signal," as recited in

claim 1. Claim 1 is thus allowable over Aiba et al. Claims 3-5 depend from claim 1 and are also allowable over Aiba et al.

Additionally, independent claim 12 recites a circuit for converting voltage levels that includes, inter alia, "a complementary inverter connectable between a first power supply providing a third voltage level and a second power supply providing a fourth voltage level, the third voltage level and the fourth voltage level being lower than the greater of the first and second voltage levels, wherein the second transistor clamps a voltage level at the node between the third voltage level and the fourth voltage level; and wherein the voltage level at the node is approximately the third voltage level in response to the first voltage level of the input signal, and approximately the fourth voltage level in response to the second voltage level." The Examiner considered Aiba et al.'s power supply line 13 as having a voltage level corresponding to Applicant's claimed first voltage level and Aiba et al.'s ground as corresponding to Applicant's claimed second voltage level. See Office Action, page 3; see also Aiba et al., page 5, paragraph [0102], and Figs. 1, 2, and 17. However, Aiba et al. does not teach, at least, "a complementary inverter coupled between a first power supply providing a third voltage level and a second power supply providing a fourth voltage level, the third voltage level and the fourth voltage level being lower than the greater of the first and second voltage levels," as recited in claim 12. Consequently, Aiba et al. also fails to teach, at least, "wherein the second transistor clamps a voltage level at the node between the third voltage level and the fourth voltage level; and wherein the voltage level at the node is approximately the third voltage level in response to the first voltage level of the input signal, and approximately the fourth voltage level in response to the

second voltage level," as recited in claim 12. Therefore, independent claim 12 is allowable over Aiba et al. Claims 13 and 15 depend from claim 12 and are also allowable over Aiba et al.

Finally, independent claim 20 recites a method for converting voltage levels that includes, inter alia, "providing a first power supply of a first voltage level; providing a second power supply of a second voltage level; providing a third power supply of a third voltage level; . . . pulling a voltage level at a node disposed between the second transistor and the current source to the third voltage level in response to the first state of the input signal." Aiba et al. at most teaches two power supplies, i.e., power supply line 13 and ground. See Aiba et al., page 5, paragraph [0102], and Figs. 1, 2, and 17. In other words, Aiba et al. fails to teach, at least, "providing a third power supply of a third voltage level." Consequently, Aiba et al. also fails to teach, at least, "pulling a voltage level at a node disposed between the second transistor and the current source to the third voltage level in response to the first state of the input signal," as recited in claim 20. Claim 20 is therefore allowable over Aiba et al. Claims 21 and 23 depend from independent claim 20 and are also allowable over Aiba et al.

Applicant also traverses the rejection of claims 20, 22, and 25 under 35 U.S.C. § 102(b) as anticipated by Fujita, because Fujita does not teach each and every element of these claims. Particularly, Fujita only teaches a voltage comparator circuit capable of comparing voltages and does not mention that the circuit has three power supplies. See Fujita, ABSTRACT and Description of the Preferred Embodiments. Therefore, Fujita fails to teach, at least, "providing a first power supply of a first voltage level; providing a second power supply of a second voltage level;

providing a third power supply of a third voltage level; . . . [and] pulling a voltage level at a node disposed between the second transistor and the current source to the third voltage level in response to the first state of the input signal," as recited in independent claim 20. Therefore, claim 20 is allowable over Fujita. Claims 22 and 25 depend from independent claim 20 and are also allowable over Fujita.

The rejection of claims 1, 2, 7, 12, and 13 under 35 U.S.C. § 102(a) as anticipated by APA is improper, because APA fails to teach each and every element of these claims.

Particularly, claim 1 recites a circuit for converting voltage levels that includes, inter alia, "a current source formed between the second transistor and the second power supply." The Examiner considered resistor 36 and transistor 38 in Fig. 2 as constituting a current source. Office Action, page 6. Applicant disagrees. A current source is known to be a device that conducts an electrical current independent of the voltage across its terminals. See http://en.wikipedia.org/wiki/Current_source. Resistor 36 and transistor 38 in Fig. 2 do not form a current source. Therefore, APA fails to teach at least "a current source formed between the second transistor and the second power supply," as recited in claim 1. Claim 1 is thus allowable over APA. Claims 2 and 7 depend from claim 1 and are also allowable over APA.

Similarly, claim 12 recites, inter alia, "a current source providing a current in response to the first voltage level of the input signal." For reasons similar to those set forth above regarding claim 1, claim 12 is allowable over APA. Claim 13 depends from claim 12 and is also allowable over APA.

Finally, regarding the rejection of claims 6, 14, and 24 under 35 U.S.C. § 103(a) as unpatentable over Aiba et al., Applicant submits that, as noted above, claims 1, 12, and 20 are not anticipated by Aiba et al. and, further, are not obvious in view of Aiba et al., at least because Aiba et al. entirely fails to disclose limitations of each of these claims. Claims 6, 14, and 24 depend from claims 1, 12, and 20 respectively, and are also allowable at least because of their dependence from an allowable base claim.

In view of the foregoing remarks, Applicant respectfully requests reconsideration and reexamination and the timely allowance of the pending claims.

If there is any fee due in connection with the filing of this Preliminary Amendment, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: August 11, 2005

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